IN THE SPECIFICATION:

Please replace paragraph [0011] of the specification with the following amended paragraphs showing changes:

[0011] Moreover, depending on the depth of the ~~pipe-line~~ pipeline, there could be several conditional branches that enter the pipeline before the first branch is resolved. Without the mispredict PC FIFO, the second branch has to be stalled until the first branch is ~~grouoped~~ grouped in GR stage. This causes the performance issues because the prefetcher can not prefetch the branch targets ~~a-head~~ ahead of time.

Please replace paragraph [0019] of the specification with the following amended paragraphs showing changes:

[0019] In one embodiment of the present invention, ~~an associated mispredict PC queue in~~ the mispredict PC storage includes a mispredict PC queue and staging registers, the mispredict PC queue having ~~has~~ at least as many registers as the number of staging registers ~~pipeline has stages~~. In an embodiment to be illustrated and described, the mispredict PC queue has one more slot than the number of staging registers, ~~pipeline has stages~~, guaranteeing that the mispredict PC queue will not overflow and lose a mispredict PC value.

Please replace paragraph [0038] of the specification with the following amended paragraph showing changes:

[0038] Though not illustrated in FIGURE 1, the DSP 100 has an overall memory architecture that 100 is typical of conventional DSPs and microprocessors. That is, its registers are fast but small; its instruction

and [[date]] data caches (contained respectively in the PFU 110 and the LSU 140) are larger, but still inadequate to hold more than a handful of instructions or data; its local instruction memory and data memory 122 are larger still, but may be inadequate to hold an entire program or all of its data. An external memory (not located within the DSP 100 itself) is employed to hold any excess instructions or data.